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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/628,941
Filing Date: July 29, 2003
Appellant(s): FRATTI ET AL.

MAILED

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GROUP 2800

Kevin M. Mason
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 12/01/2005 appealing from the Office action mailed 09/02/2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,091,121	Oda	7-2000
6,559,011	Shibib	5-2003

Savastiouk et al., "Atmospheric downstream plasma", European semiconductor, June 1998, pages 1-4.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oda in view of Savastiouk et al. and Shibib.

Regarding claims 1, 3, 13 and 16, Oda teaches in figures 1-2 and related text a method for controlling curvature of a transistor device comprising a device film 4 formed on a substrate 1, the method comprising the steps of:

applying a stress compensation layer (e.g. any of layers 12, 15, 17) to a surface of the device film 4 (or any other layer below them), the stress compensation layer having a tensile stress (Oda: column 6, lines 44-45 and column 8, lines 49-52) sufficient to counterbalance at least a portion of the overall residual stress of the device.

Oda does not teach thinning the substrate, wherein a power transistor device having an overall residual stress attributable at least in part to the thinning step.

Savastiouk et al. teach thinning (backgrinding) the substrate (page 1, paragraphs 1-4). Shibib teaches a DMOS power transistor (column 7, lines 9-25).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the device in a power transistor application and to thin the substrate in Oda's device in order to use the device in an application which requires a power transistor and in order to adapt the device to current technology and to increase the numbers of chips per wafer, respectively. The combination is motivated by the teachings of Savastiouk et al. who point out the advantages of using thinner substrate (backgrinding the substrate, page 1, paragraphs 1-4).

Regarding the claimed limitations of a device having an overall residual stress attributable at least in part to the thinning step, these features are inherent in prior art's device, because thinning the device inherently causes an overall residual stress.

Regarding claims 2, 4-6, 8-10 and 14-15, prior art's device includes a stress compensation layer comprises a thin film (a thin film is a relative term), wherein the device substrate is thinned using aggressive backside substrate removal processing, wherein the thin film comprises a dielectric material comprising at least one of a silicon nitride, a silicon oxide, a silicon oxynitride, an oxynitride, a nitride and combinations comprising at least one of the foregoing dielectric materials (Oda: column 6, lines 44-45 and column 8, lines 49-52), wherein the thin film is applied using a deposition technique comprising at least one of sputtering, chemical vapor deposition, electroplating and spin-on processing, wherein the thin film serves as an encapsulating layer, wherein the

stress compensation layer applied to the surface of the device changes and maintains the curvature of the device (this feature is inherent in prior art's device).

Regarding claims 7 and 11-12, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to monitor the curvature of the device by using an off-axis optical laser technique, and to repeat the steps of thinning and applying until a desired curvature is attained in prior art's device in order to have better control over the characteristics of the device and by using known monitoring techniques.

(10) Response to Argument

Appellant argues that prior art does not teach a stress compensation layer with a tensile stress sufficient to counterbalance at least a portion of an overall residual stress of a power transistor device, as recited in claims 1, 13 and 16, because layers 12, 15 and 17 of Oda do not have a tensile stress sufficient to counterbalance any portion of an overall residual stress resulting from substrate thinning. Appellant further argues that layers 12, 15 and 17 of Oda are protecting nitride films, and the protecting insulator film of Oda is merely present to compensate for stresses inherent in layers adjacent thereto.

Appellant describes a device comprising a dielectric film formed over a device film, wherein a thinning process was applied to the substrate (see e.g., claims 13 and 16). Appellant calls the dielectric film "stress compensation layer" (see specification, page 9, lines 7-16), and states that the "stress compensation layer" can comprise any

one of a silicon nitride, a silicon oxide, a silicon oxynitride, an oxynitride, a nitride and combinations comprising at least one of the foregoing dielectric materials. Appellant further states that the tensile stress of the "stress compensation layer" is sufficient to counterbalance at least a portion of an overall residual stress of the device.

Appellant does not disclose any difference between the dielectric film (formed e.g. of silicon nitride) called "stress compensation layer", and a dielectric film (also formed e.g. of silicon nitride) used in Oda's device or in any other semiconductor device. The fact that appellant calls the claimed dielectric film "stress compensation layer", does not distinguish it from Oda's dielectric film and does not create any structural differences between the "stress compensation layer" and any other dielectric film which comprises silicon nitride. Therefore, it appears that any semiconductor device having a dielectric film formed e.g. of silicon nitride, and inherently having a tensile stress, can be called "stress compensation layer", and when formed on a "device film", will inherently produce a tensile stress sufficient to counterbalance at least a portion of an overall residual stress of the device.

Furthermore, appellant states that the "stress compensation layer" has a tensile stress sufficient to counterbalance any portion of an overall residual stress resulting from substrate thinning. Oda also teaches a dielectric film (12, 15 and 17) having a tensile stress (column 6, lines 44-45 and column 8, lines 49-52). This tensile stress must inherently counterbalance at least a portion of an overall residual stress in the device. Even appellant admits that Oda's protecting insulator film counterbalances a portion of an overall residual stress in the device ("insulator film....compensate for

stresses inherent in layers adjacent thereto", appeal brief, page 5, second paragraph, last sentence). Therefore, layers 12, 15 and 17 of Oda have a tensile stress sufficient to counterbalance any portion of an overall residual stress, as claimed.

Regarding appellant's argument that layers 12, 15 and 17 of Oda do not have a tensile stress sufficient to counterbalance any portion of an overall residual stress resulting from substrate thinning, the combined device of Oda, Savastiouk et al. and Shibib provides a structure wherein a thinning process was applied to the substrate. The thinning process is known to cause tensile stress (see specification, page 4, lines 7-12, and Savastiouk et al., page 1, paragragh 3 and 9), which in turn creates voids and warping of the substrate (see specification, page 3, lines 20-24, and Savastiouk et al., page 1, paragragh 3 and 9). Therefore, thinning Oda's device would inherently result in a device having an overall residual stress attributable at least in part to the thinning step.

Appellant argues that there is no motivation to combine Savastiouk et al. with Oda, because although Savastiouk et al. teach an advantage for thinning a substrate, Savastiouk et al. do not disclose or suggest that thinner wafers may be used to control curvature of a power transistor device, as taught by the present invention.

Thinner wafers are not used to control curvature of a power transistor device. Curvature of a device is the result of thinning the wafer. Controlling the curvature of a device is done by forming a dielectric film over the device film. Furthermore, there is

motivation to combine Savastiouk et al. with Oda, because Oda does not teach thinning a substrate, and Savastiouk et al. teach the advantages for thinning a substrate.

Appellant argues that an artisan would not be motivated to combine Oda with Savastiouk et al., because although Savastiouk et al. recite "residual stress" and "thinning," Savastiotzk does not suggest that the overall residual stress of a device is attributable to the thinning step.

Thinning (grinding) a substrate is known to create tensile stress, which in turn causes warping of the substrate (see specification, page 4, lines 7-12, and Savastiouk et al., page 1, paragragh 3 and 9). Therefore, thinning a substrate would inherently result in a device having an overall residual stress attributable at least in part to the thinning step. Savastiouk et al. teach on page 1, paragraph 3 that as a result of backgrinding (i.e. thinning), "residual stress caused wafer bow and warp". Therefore, Savastiouk et al. explicitly state that the overall residual stress of a device is attributable to the thinning step. In any event, Savastiouk et al. do not need to teach a phenomenon which naturally occurs when a substrate is thinned or grinned.

Appellant argues that prior art does not teach thinning the substrate and applying a stress compensation layer are performed repeatedly until a desired curvature is attained, as recited in claim 7, because the cited references do not disclose that thinning of the substrate would produce a curvature of the device.

As discussed above, thinning (grinding) a substrate is known to inherently create tensile stress, which in turn causes warping of the substrate. Furthermore, Savastiouk et al. teach on page 1, paragraph 3 that the result of backgrinding, "residual stress caused wafer bow and warp".

Appellant argues that prior art does not suggest a stress compensation layer applied to the surface of the device changes or maintains the curvature of the device, as recited in claims 9 and 10.

As discussed above, it is well known that tensile stress causes a curvature of a device. A dielectric film, or "stress compensation layer", inherently produces tensile stress. Therefore, when the dielectric film is formed on a surface of the device it applies tensile stress to the device, and this tensile stress affects (changes or maintains) the curvature of the device.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

O.N.

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